BU9-98-110DIV
09/666,325

21. (Currently Amended) A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper percentage above 10% to 20% of said bonding pad comprises a silicided surface, and

wherein a thickness of said [uppermost layer] top level of metallurgy reduces sensitivity to resistivity shifts associated with said silicided surface.

22. (Previously Presented) The semiconductor device in claim 21, wherein a bottom 80% to 90% of said bonding pad is free of silicide.

23. (Previously Presented) The semiconductor device in claim 22, wherein said silicided surface is free of oxides and silicide islands.

24. (Previously Presented) The semiconductor device in claim 23, wherein, prior to formation of said silicided surface, said bonding pad is cleaned by applying one of an ammonia plasma and a hydrogen plasma to make said bonding pad free of said oxides and silicide islands.

25. (Currently Amended) [The semiconductor device in claim 21], A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,

wherein a thickness of said top level of metallurgy reduces sensitivity to resistivity shifts associated with said silicided surface, and

wherein said semiconductor device further [comprising] comprises a terminal connected to said bonding pad,

wherein a thickness of said silicided surface increases adhesion between said terminal and said bonding pad.

26. (Previously Presented) The semiconductor device in claim 25, wherein said terminal comprises one of a lead and tin solder.

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27. (Cancelled).

28. (Previously Presented) The semiconductor device in claim 21, wherein said top level of metallurgy comprises copper.

29. (Currently Amended) A semiconductor chip comprising:

an exterior surface having a top level of metallurgy; and

an interior having at least one internal level of metallurgy,

wherein said top level of metallurgy is thicker than said internal level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper percentage above 10% to 20% of said bonding pad comprises a silicided surface, and

wherein a thickness of said [uppermost layer] top level of metallurgy reduces sensitivity to resistivity shifts associated with said silicided surface.

30. (Previously Presented) The semiconductor device in claim 29, wherein a bottom 80% to 90% of said bonding pad is free of silicide.

31. (Previously Presented) The semiconductor device in claim 30, wherein said bonding pad is free of oxides and silicide islands.

32. (Previously Presented) The semiconductor device in claim 31, wherein, prior to formation of said silicided surface, said bonding pad is cleaned by applying one of an ammonia plasma and a hydrogen plasma to make said bonding pad free of said oxides and silicide islands.

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33. (Currently Amended) [The semiconductor device in claim 29,] A semiconductor chip comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,

wherein a thickness of said top level of metallurgy reduces sensitivity to resistivity shifts associated with said silicided surface, and

wherein said semiconductor device further [comprising] comprises a terminal connected to said bonding pad, wherein a thickness of said silicided surface increases adhesion between said terminal and said bonding pad.

34. (Previously Presented) The semiconductor device in claim 33, wherein said terminal comprises one of a lead and tin solder.